REMARKS

This application has been carefully reviewed in light of the Office Action dated April 23, 2009. Claims 1, 4, 7, 8 and 9 are in the application, with Claim 1 being independent. Claim 1 has been amended herein. Reconsideration and further examination are respectfully requested.

The title of the invention was objected to as allegedly not being descriptive. Without conceding to the correctness of the rejection, the title has been amended herein, as suggested by the Examiner. Withdrawal of this rejection is respectfully requested.

The drawings were objected to for allegedly not showing every feature of the invention specified in the claims. In particular, the Office Action took the position that the claimed cross-bar switch was not shown in the drawings. Without conceding to the correctness of the objection, Claim 1 has been amended herein to recite a cross-bar switch comprising at least a first interface connected to a memory controller and a second interface connected to a processor bus.

Applicants respectfully submit that the claimed cross-bar switch comprising at least a first interface connected to a memory controller and a second interface connected to a processor bus is shown in at least Figures 1 and 2. In this regard, the cross-bar switch is depicted in Figures 1 and 2 as system bus bridge 106. For example, as discussed at page 7, lines 15 to 18 of the specification, system bus bridge 106 corresponds to a cross-bar switch. As shown in Figures 1 and 2, the cross-bar switch 106 includes a first interface which is connected to memory controller 105 and a second interface which is connected to CPU bus 108.

Accordingly, reconsideration and withdrawal of this objection are

respectfully requested.

Claims 1 to 4 and 7 to 9 were rejected under U.S.C. § 112, first paragraph for alleged failure to comply with the written description requirement. Without conceding to the correctness of the rejection, Claim 1 has been amended herein to recite a cross-bar switch comprising at least a first interface connected to a memory controller and a second interface connected to a processor bus, wherein the external processor connected to the external bus interface can use the processor bus and the second interface of the cross-bar switch, and wherein the built-in processor can use the processor bus and the second interface of the cross-bar switch.

Applicant respectfully submits that support for these features can be found at least in Figures 1 and 2 and their accompanying descriptions in the specification. For example, as shown in Figures 1 and 2 and discussed on page 4 of the specification at lines 25 to 27, system bus bridge 106 has a first interface which is connected to MCBus 110 which is a connection bus of the memory controller 105, in addition to a second interface which is connected to CPU bus 108. Furthermore, as also shown in Figures 1 and 2 and discussed on page 4, CPU 102 uses the CPU bus 108, and uses the second interface of system bus bridge 106 to connect to the system bus bridge 106 through CPU bus 108. In addition, external CPU 103 is connected to the external bus interface 104 and uses the CPU bus 108. By using CPU bus 108, the external CPU 103 connected to the external bus interface 104 uses the second interface of system bus bridge 106 to connect to the system bus bridge 106.

In view of the foregoing, Applicant respectfully submits that the claims find full support in the original specification, and withdrawal of the rejection under § 112, first

paragraph, is respectfully requested.

Claims 1 and 7 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 4,065,809 (Matsumoto), in view of U.S. Patent No. 4,521,852 (Guttag). In addition U.S. Patent No. 5,214,775 (Yabushita) was used as "evidence for showing that processors on separate chips may share a memory found on one of the chips". Claims 4, 8 and 9 were rejected under 35 U.S.C. § 103(a) over Matsumoto in view of Guttag, and further in view of the Examiner's taking of Official Notice.

The present claims are directed to a processor system. According to one aspect, a cross-bar switch includes at least a first interface connected to a memory controller and a second interface connected to a processor bus, in which the second interface of the cross-bar switch is shared via the processor bus between an external bus interface and a built-in processor. When a first enable signal is asserted in addition to a second enable signal being deasserted, the built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external processor connected to the external bus interface can use the processor bus and the second interface of the cross-bar switch exclusively. On the other hand, when the second enable signal is asserted while the first enable signal is deasserted, the external bus interface is in a reset state to suppress issuance of a request for using the processor bus from the external processor connected to the external bus interface and the built-in processor can use the processor bus and the second interface of the cross-bar switch exclusively without stopping an operation of the external processor.

By virtue of this arrangement, it is ordinarily possible to connect the built-n processor and the external processor to the cross-bar switch via the same interface of the

cross-bar switch, namely the second interface. Accordingly, the number of bus connection interfaces of the cross-bar switch can ordinarily be reduced, in turn reducing circuit scale and cost. In addition, it is ordinarily possible to suppress the issuance of a request for using the processor bus from the external processor by asserting a second enable signal in addition to deasserting a first enable signal, without stopping operation of the external processor. Furthermore, it is ordinarily possible to suppress issuance of a request for using the processor bus from the built-in processor by asserting a first enable signal and deasserting a second enable signal.

Turning to specific claim language, amended independent Claim 1 is directed to a processor system including a single semiconductor substrate on which is provided a built-in processor, a memory controller, an external bus interface to which an external processor is connected from outside of the single semiconductor substrate, a processor bus which is connected with the built-in processor and the external bus interface, and a cross-bar switch that mutually connects the memory controller and the processor bus. The cross-bar switch comprises at least a first interface connected to the memory controller and a second interface connected to the processor bus. First and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively. The first enable signal is asserted while the second enable signal is deasserted, so that the built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external processor connected to the external bus interface can use the processor bus and the second interface of the cross-bar switch exclusively. On the other hand, the second enable signal is asserted while the first enable signal is deasserted, so that the external bus

interface is in a reset state to suppress issuance of a request for using the processor bus from the external processor connected to the external bus interface and the built-in processor can use the processor bus and the second interface of the cross-bar switch exclusively, without stopping an operation of the external processor.

The applied references, alone or in any permissible combination, are not seen to disclose or suggest the subject matter of Claim 1.

In particular, none of Matsumoto, Guttag and Yabushita are seen to disclose or suggest at least the claimed features of (i) a processor bus which is connected with the built-in processor and the external bus interface to which an external processor is connected, and a cross-bar switch that mutually connects the memory controller and the processor bus, wherein the cross-bar switch comprises at least a first interface connected to the memory controller and a second interface connected to the processor bus, (ii) the first enable signal being asserted while the second enable signal is deasserted, so that the built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external processor connected to the external bus interface can use the processor bus and the second interface of the cross-bar switch exclusively, and (iii) the second enable signal being asserted while the first enable signal is deasserted, so that the external bus interface is in a reset state to suppress issuance of a request for using the processor bus from the external processor connected to the external bus interface and the built-in processor can use the processor bus and the second interface of the cross-bar switch exclusively, without stopping an operation of the external processor.

Matsumoto describes a system including a CPUa 11 and a CPUb 12, where

the CPUa 11 is prevented from producing a read-write signal R/Wa 26 by setting the logic level for the signal WAITa 25 to "1". CPUb 12 is similarly prevented from producing an independent read-write signal R/Wb 44 by setting the logic level for the signal WAITb 41 to "1".

The Office Action took the position that the first and second enable signals recited in the present Claim 1 are disclosed by Matsumoto. However, Applicant respectfully submits that the cited portions of Matsumoto merely describe that CPUa 11 is prevented from producing read-write signal R/Wa 26 as long as one signal, namely signal WAITa 25, is set at "1". On the other hand, CPUa 11 can generate signal R/Wa 26 only after the signal WAITa 25 is set at "0". Matsumoto, column 4, lines 49 to 63. Similarly, as discussed at column 6, lines 42 to 38, CPUb 12 does not issue a read-write signal R/Wb 44 so long as one signal, namely signal WAITb 41, continues to have a logic level of "1". Thus, CPUb 12 is kept in a waiting position until signal WAITb 41 is set to "0".

In contrast, Claim 1 recites asserting a first enable signal while deasserting a second enable signal, so that the built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external processor connected to the external bus interface can use the processor bus and the second interface of the cross-bar switch exclusively, and asserting the second enable signal while deasserting the first enable signal, so that the external bus interface is in a reset state to suppress issuance of a request for using the processor bus from the external processor connected to the external bus interface and the built-in processor can use the processor bus and the second interface of the cross-bar switch exclusively, without stopping an operation of the external processor.

Moreover, the Office Action conceded that Matsumoto does not disclose a cross-bar switch, and asserted that it would be obvious to use such a cross-bar switch in the system disclosed by Matsumoto. Applicant respectfully requests a citation in support of this feature.

Furthermore, even if such a cross-bar switch were somehow used in the system disclosed by Matsumoto, Applicant respectfully submits that the combination would still fail to teach the claimed arrangement. In particular, Claim 1 recites a cross-bar switch with two interfaces, in which the same interface of the cross-bar switch is shared via a common processor bus by the external processor and the built-in processor. Accordingly, Applicant respectfully submits that even if Matsumoto was modified to include a cross-bar switch, the combination would fail to teach the claimed utilization of two interfaces thereof, in which a first interface is connected to a memory controller and a second interface is shared via a common processor bus by an external processor and a built-in processor.

Guttag and Yabushita have been studied but are not seen to overcome the deficiencies of Matsumoto.

Accordingly, Matsumoto, Guttag and Yabushita are not seen to disclose or suggest at least the claimed features of (i) a processor bus which is connected with the built-in processor and the external bus interface to which an external processor is connected, and a cross-bar switch that mutually connects the memory controller and the processor bus, wherein the cross-bar switch comprises at least a first interface connected to the memory controller and a second interface connected to the processor bus, (ii) the first enable signal being asserted while the second enable signal is deasserted, so that the

built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external processor connected to the external bus interface can use the processor bus and the second interface of the cross-bar switch exclusively, and (iii) the second enable signal being asserted while the first enable signal is deasserted, so that the external bus interface is in a reset state to suppress issuance of a request for using the processor bus from the external processor connected to the external bus interface and the built-in processor can use the processor bus and the second interface of the cross-bar switch exclusively, without stopping an operation of the external processor.

In light of the deficiencies of the applied art, Applicant respectfully submits that Claim 1 is in condition for allowance and respectfully requests the same.

The other claims in the application are each dependent from the independent claim and are believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

No other matters being raised, it is believed that the entire application is fully in condition for allowance, and such action is courteously solicited.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office by telephone at (714) 540-8700. All correspondence should be directed to our address given below.

Respectfully submitted,

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